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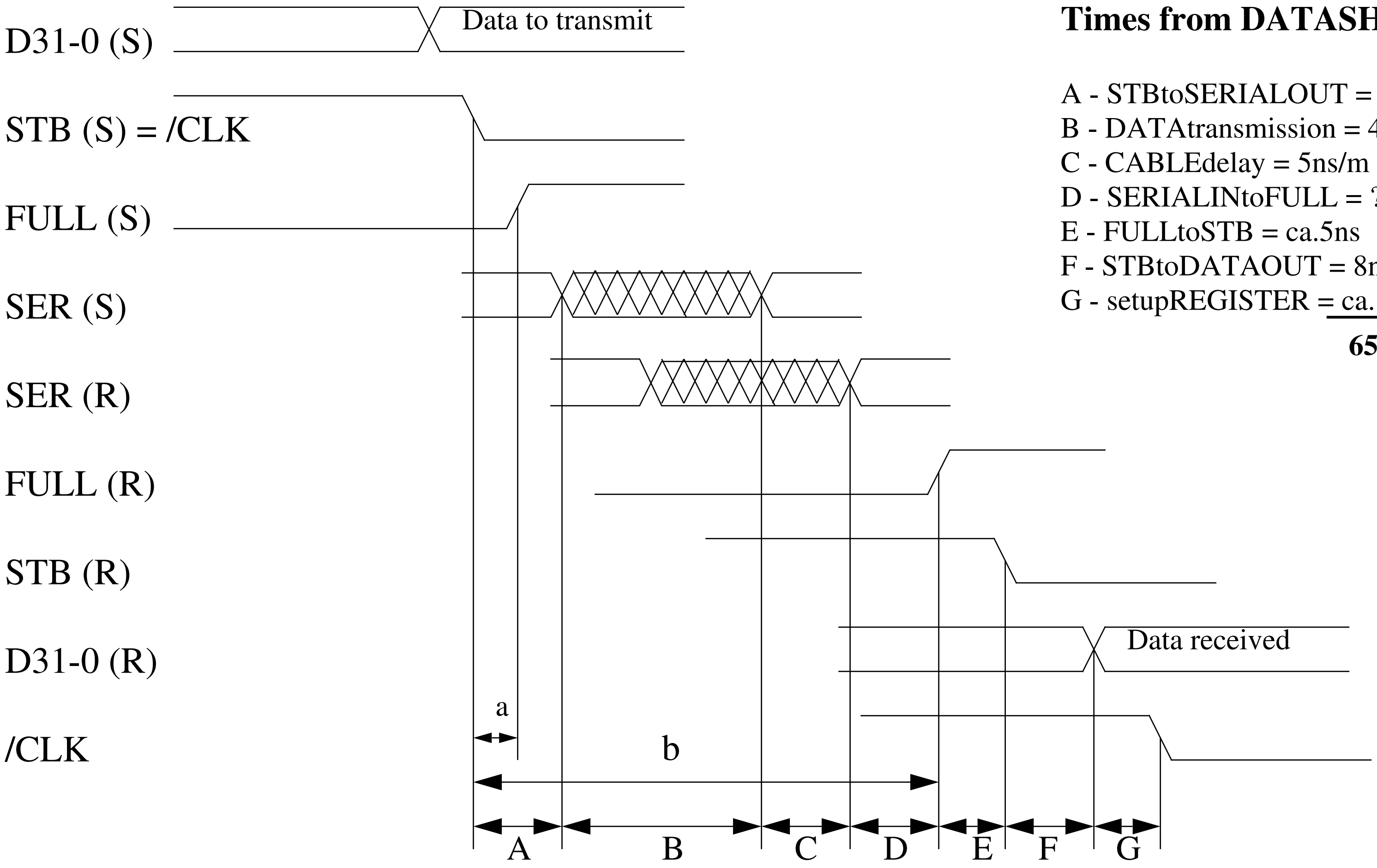
Delays in synchronous data transmission via AutoBahn



Times from DATASHEETs:

A - STBtoSERIALOUT = ?
B - DATAtransmission = 40ns
C - CABLEdelay = 5ns/m
D - SERIALINtoFULL = ?
E - FULLtoSTB = ca.5ns
F - STBtoDATAOUT = 8ns
G - setupREGISTER = ca. 2ns

65ns+X

H. Leich

APE Workshop - Frascati 1997

Modes of Operation

1. Transmit: Sending data from SRAM to AutoBahn: SRAM --> AutoBahn

2. Receive: Reading data from AutoBahn and writing to SRAM: AutoBahn --> SRAM

3. Receive&Compare: Reading data from AutoBahn and comparing with data from SRAM in hardware: AutoBahn == SRAM

Comments:

- In all modes VME access to SRAM can be carried out only when sending/ receiving AutoBahn interfaces are inactive

- Data are transmitted and received from/to SRAM under control of a built-in DMA unit

- In modes 1..3 Error- and Block-Counters are handled inside the Control FPGA. Error flags can be read out at any time via the VME-interface
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Measurements with AEB Board:

- with 50cm cable:

  b1: TxSTB-to-RxFULL = 85ns (first data word)
  bn: TxSTB-to-RxFULL = 70ns (all other data words; device runs below max. transmission speed
  bn: TxSTB-to-RxFULL = 40ns (all other data words; device runs at max. transmission speed

- with 3 m cable:

  b1: TxSTB-to-RxFULL = 100ns (first data word)
  bn: TxSTB-to-RxFULL = 85ns (all other data words; device runs below max. transmission speed)
  bn: TxSTB-to-RxFULL = 40ns (all other data words; device runs at max. transmission speed

AutoBahn Evaluation Board

- Designed for evaluation of AutoBahn based point-to-point links
- Incorporates a VME slave interface thus it can be used as an VME to AutoBahn interface module
- Access to the 4 AutoBahn interfaces is via a synchronous SRAM (Pentium Cache RAM)