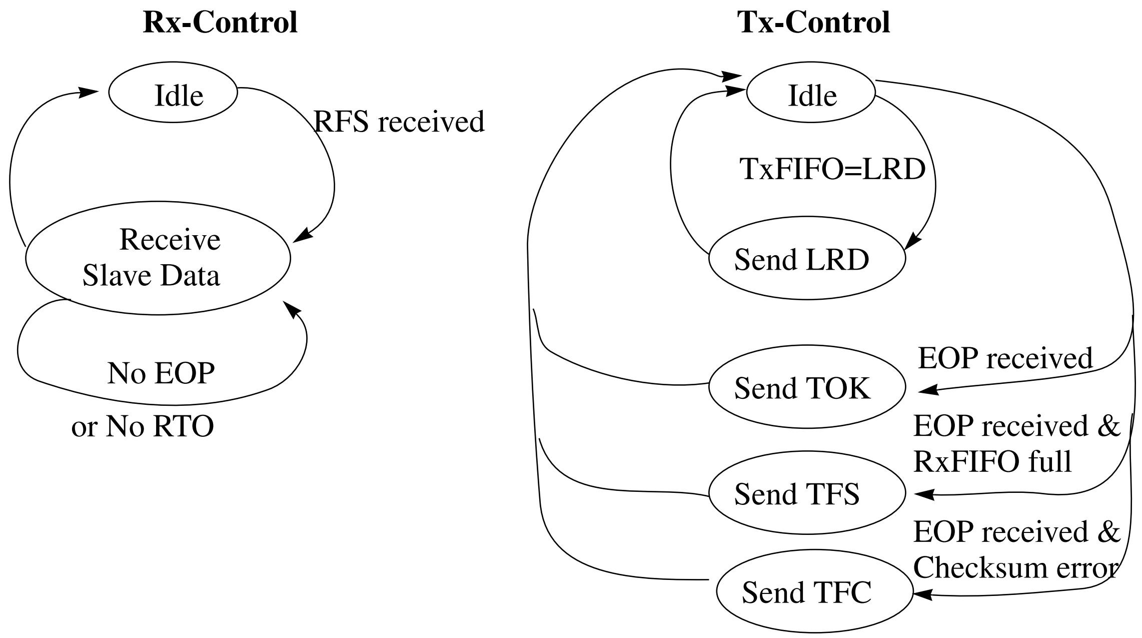
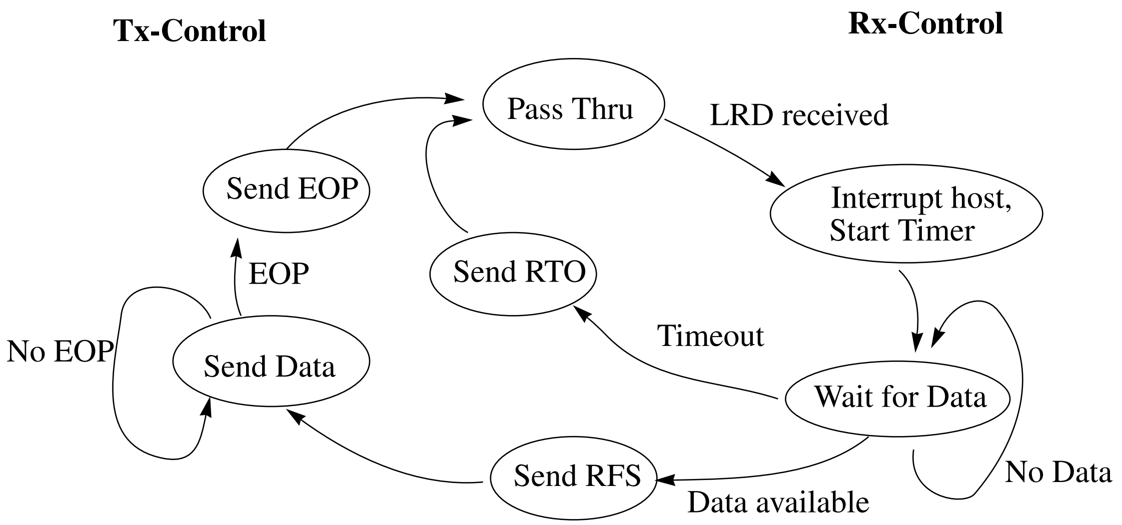
## LRD - Local Read

The master sends: LRD
The Slave recognizes LRD command and writes a RFS DATA EOP data-stream. If no data available (TxFIFO is empty), the Slave signals (Interrupt) the Master request to his host and starts the timeout down counter.
When the Timeout counter reaches zero and the TxFIFO is still empty, a RTO status message will be sent. If the Master receive an EOP, he sends a TOK, TFS or TFC to the Slave.

## Master states




## Slave states

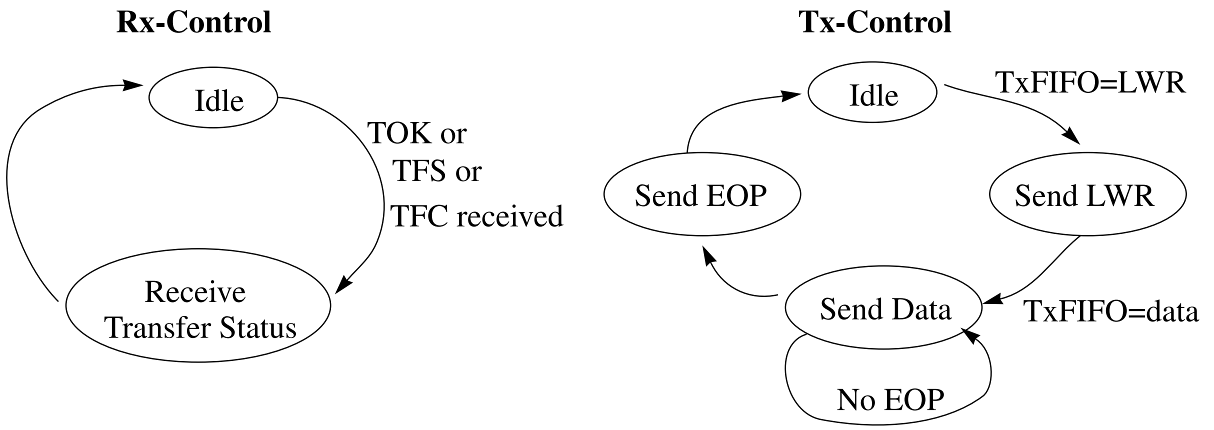


# Command Implementation (examples):

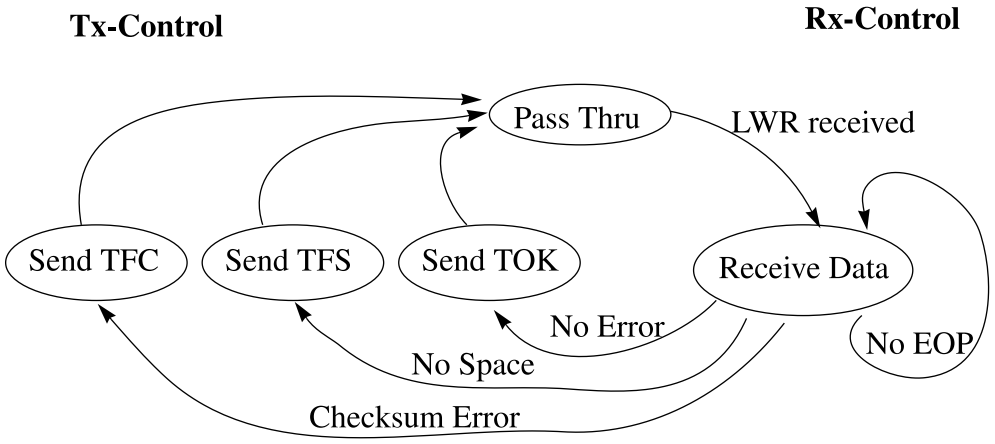
## LWR - Local Write

The master sends: LWR data ... EOP
The data sent, are received and passed through by all modules until the destination modul is arrived.
After receiving EOP followed by the checksum, the slave sends back its transfer status.
The software of the master PC has to read its RxFIFO to handle the transfer status.

### Master states




### Slave states



| *Abbr.* | *Code* | *Description* | *Used by* |
|---|---|---|---|
| **DNC** | 0 | Data, No Control, the 0xffffffff word is a data word | master / slave |
| **GWR** | 1 | Header, Global Write (Broadcast)<br>followed by 32 Bit Packet No. + Packet Length | master |
| **LWR** | 2 | Header, Local Write<br>followed by 32 Bit Packet No. + Packet Length | master |
| **GRD** | 3 | Header, Global Read | master |
| **LRD** | 4 | Header, Local Read | master |
| **RFS** | 5 | Header, Read From Slave<br>followed by 32 Bit Packet No. + Packet Length | slave |
| **EOP** | 6 | End Of Packet,<br>followed by a Checksum (32 bit XOR) | master/ slave |
| **EOG** | 7 | End Of Global transfer | master |
| **TOK** | 8 | Transfer o. k. | master / slave |
| **TFS** | 9 | Transfer failed, no Space(FIFO full) | master / slave |
| **TFC** | 10 | Transfer failed, Checksum error | master / slave |
| **RTO** | 11 | Read Timeout | slave |
| **WHO** | 12 | Registration of all Slaves in the ring | master |
| **GRES** | 13 | Global Reset | master |
| **LRES** | 14 | Local Reset | master |
| **GNT** | 15 | Grant, Master token | master |

# PCI to AutoBahn Interface

## Data Transfer Principles:

In the ring structure one Master is connected to one or more Slaves. Each interface modul (Master and Slave) has two buffers, one for receiving data (RxFIFO) and one for transmitting data (TxFIFO). Because of this FIFO structure it is possible to pipe data together with Control/Status information.

Data is transferred in form of packets. Each packet is framed by a Header and an End Of Packet (EOP) terminator.

## Transfer protocol:

**Problem:** distinguish between Data and Control information
**Solution:** Word Stuffing using the code 0xffffffff

If in the data stream the code 0xffffffff is detected then:

```
if  NEXT_DATA == 0x00xxxxxx
       then PREVIOUS_DATA is DATA (0xffffffff)
       else  NEXT_DATA is COMMAND/STATUS information
```

Thus, Command and Status messages consist of at least two 32 Bit words, the first word being 0xffffffff, the second word carrying the status or control information. The encoding and decoding of 0xffffffff-data and all commands/status messages is completely done by hardware.

## Control and Status messages:

### Command/message formats:

| DNC #0 | not used |
|---|---|
| 31 24 | 23 0 |

| | MASTER address | | SLAVE address | |
|---|---|---|---|---|
| code #1 .. 15 | X5............X0 | Y5............Y0 | X5...........X0 | Y5...........Y0 |
| 31 24 | 23 18 | 17 12 | 11 6 | 5 0 |

| PACKET No. | PACKET Length (bytes) | |
|---|---|---|
| N15..........................................................N0 | L15..................................L2 | 0 0 |
| 31 16 | 15 | 0 |